

## REMARKS

Claims 1-21 remain in the present application. Applicants respectfully request further examination and reconsideration of the rejections based on the above amendments and the arguments set forth below.

### Claim Objections

Claims 2 and 13 are objected to by the above referenced Office Action with respect to the cited terms "memory" and "register." Applicants point out that as in common usage by those skilled in the art, the term "memory" is a term referring generally to many different types of storage for a digital system. The term "register" is a more specialized term generally referring to high-speed memory within a processor or other electronic device, used to hold data for a particular purpose.

### 35 U.S.C. Section 112 rejections

Claims 6 and 17 have been amended to obviate the cited 35 U.S.C. Section 112 rejections.

### 35 U.S.C. Section 103 rejections

The above referenced Office Action rejects independent Claims 1, 10 and 12 as being unpatentable over U.S. Patent No. 6,202,044 (hereafter Tori). Applicants respectfully traverse, and point out that independent Claims 1,

10, and 12 have been amended to more particularly point out aspects of the present invention.

Embodiments of the claimed invention disclose a synchronized boot process for an In-Circuit Emulator system. Independent Claim 1 recites a microcontroller operated in lock-step synchronization with a virtual microcontroller. During a boot process, the microcontroller executes a set of boot code. In the virtual microcontroller a set of timing code is executed that is timed to take the same number of clock cycles as the microcontroller uses to execute the boot code. The boot code is stored within the microcontroller and at least one portion of the boot code is inaccessible to the virtual microcontroller.

In this manner, the synchronized boot is accomplished by running boot code in the real microcontroller while the virtual microcontroller runs dummy code with the same timing as the boot code, and this is implemented even though at least one portion of the boot code is inaccessible (e.g., hidden) to the virtual microcontroller. Registers and memory contents are then copied from the real microcontroller to the virtual microcontroller to complete initialization and enter a state of readiness for lock-step operation.

Applicants point out that this is different from the emulation system disclosed in Tori. Tori does not show, disclose, or suggest the fact that

certain boot code of the real microcontroller is not accessible to the virtual microcontroller, or to the ICE system. Such code can be, for example, various initialization processes that contain proprietary information such as serial numbers, passwords, and the like, that should not be exposed. These limitations are not shown, disclosed, or suggested by Tori.

With respect to Official Notice being taken with regard to the “hiding of data”, Applicants assert that the maintaining of lockstep synchronization between a real microcontroller and a virtual microcontroller during a boot process, where circuitry comprising the virtual microcontroller is simulated, and thus may not be exactly the same as the circuitry comprising the real microcontroller, is not obvious or well known in the art. As described in the specification of the present application at, for example, page 26 lines 3-29, the real microcontroller includes circuitry that must be initialized (e.g., clocks, amplifiers, analog components, etc.) which are not incorporated in the virtual microcontroller. Furthermore, with respect to hidden boot code, as recited in the claimed invention, special boot code (e.g., supervisory ROM) must be kept within the boundaries of the real microcontroller and is thus inaccessible outside the chip (e.g., hidden). Applicants assert that maintaining lockstep synchronization in view of these challenges is not obvious or well known.

Accordingly, for the rationale described above, Applicants assert that the claimed invention as recited in independent Claims 1, 10 and 12 is not rendered obvious by Tori and any "Official Notice" within the meaning of 35 U.S.C. Section 103.



### CONCLUSION

Applicants respectfully assert that all claims (Claims 1-21) are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

Dated: 8/5, 2005

Glenn Barnes  
Registration No. 42,293

Two North Market Street  
Third Floor  
San Jose, CA 95113  
(408) 938-9060